PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q78894
Sung-kyu CHOI	
Appln. No.: 10/758,040	Group Art Unit: 2111
Confirmation No.: 6125	Examiner: Christopher E. LEE
Filed: January 16, 2004	

For: APPARATUS AND METHOD FOR CONNECTING PROCESSOR TO BUS

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

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I. REAL PARTY IN INTEREST

The real party of interest in this appeal is SAMSUNG ELECTRONICS CO., LTD.

Assignment of the application was submitted in the U.S. Patent and Trademark Office on January 16, 2004, and recorded on the same date at Reel 014899, Frame 0124.

II. RELATED APPEALS AND INTERFERENCES

There are no know appeals or interferences that will affect, be directly affected by, or have a bearing on the Board's decision in the pending Appeal.

III. STATUS OF CLAIMS

Claims 1-10 are all the claims pending in the application and the subject of this appeal. Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bourke et al. (U.S. Patent No. 5,509,124, hereafter "Bourke") in view of Barrenscheen et al. (U.S. Patent Application Publication No. 2003/0084226, hereafter "Barrenscheen"). Claims 2-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki et al. (JP 2000-92365A, hereafter "Masayuki") in view of Barrenscheen. Claims 7-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen, and further in view of Sodos (U.S. Patent No. 5,239,651). Claim 10 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen and Luo et al. (U.S. Patent No. 6,265,885, hereafter "Luo"). All of the claims are set forth in the attached Appendix.

IV. STATUS OF AMENDMENTS

No claim amendments were requested subsequent to the January 18, 2007 Office Action.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a buffering apparatus. Claim 1 requires an asynchronous data bus write unit (for example 921 FIG. 9) which, when control information indicating a request for writing in a buffer (for example 92) connected to an asynchronous data bus (for example FIG. 9) not synchronized with a processor is provided by a multiplexer (for example 91) connected to the processor (FIG. 6), receives third data from the multiplexer (for example 91), stores the third data, and transfers the stored third data to a second memory through the asynchronous data bus (for example paragraph [88]).

Claim 1 further requires an asynchronous data bus read unit (for example 922 FIG. 9) which, when control information indicating a request for reading from the buffer is provided by the multiplexer, receives fourth data from the second memory through the asynchronous data bus, stores the fourth data, and transfers the stored fourth data to the multiplexer (for example paragraph [89]), wherein the multiplexer (for example 91) receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor (for example paragraph [39])].

Independent claim 2 is directed to a processor bus connection method, wherein (a) when address information indicating an address of a first memory (for example 23, FIG. 1) connected to a synchronous data bus synchronized with a processor (for example 21), from the processor is received, receiving first data from the processor and transferring the received first data to the first

memory through the synchronous data bus, or receiving second data from the first memory (for example 23) through the synchronous data bus and transferring the received second data to the processor (for example, paragraphs [38] and [39]), and (b) when address information indicating an address of a second memory (for example 28) connected to an asynchronous data bus not synchronized with the processor, from the processor is received, receiving third data from the processor, transferring the third data, storing the transferred third data, and transferring the stored third data to the second memory (for example 23) through the asynchronous data bus, or receiving fourth data from the second memory through the asynchronous data bus, storing the fourth data, transferring the stored fourth data, receiving the transferred fourth data, and transferring the received fourth data to the processor (for example paragraphs [38] to [42]).

Independent claim 4 is directed to a synchronous bus and asynchronous bus path method. Claim 4 requires (a) receiving input data and transferring the received input data through a synchronous bus synchronized with a processor (for example, paragraphs [53] to [54]); (b) receiving the input data through the synchronous bus and transferring the received input data (for example paragraphs [54]); (c) generating first data or third data from the transferred input data and transferring the generated first or third data (for example, paragraphs [53] to [54]); (d) receiving the first data, transferring the received first data to a first memory through the synchronous data bus, or receiving and storing the third data and transferring the stored third data to a second memory through an asynchronous bus not synchronized with the processor (for example paragraph [55]); (e) receiving the first data through the synchronous bus and storing the

first data (for example, paragraphs [58] to [61]); and (f) receiving the third data through the asynchronous bus and storing the third data (for example, paragraphs [58] to [61]).

Independent claim 10 requires a tangible computer readable recording medium including a computer program having instructions for controlling a synchronous bus and asynchronous bus, the instructions comprising (a) receiving input data and transferring the received input data through the synchronous bus synchronized with a processor (for example, paragraphs [53] to [54]); (b) receiving the input data through the synchronous bus and transferring the received input data (for example paragraphs [54]); (c) generating first data or third data from the transferred input data and transferring the generated first or third data (for example, paragraphs [53] to [54]); (d) receiving the first data, transferring the received first data to a first memory through the synchronous data bus, or receiving and storing third data and transferring the stored third data to a second memory through an asynchronous bus not synchronized with the processor (for example paragraph [55]); (e) receiving the first data through the synchronous bus and storing the first data (for example, paragraphs [58] to [61]); and (f) receiving the third data through the asynchronous bus and storing the third data (for example, paragraphs [58] to [61]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Rejection of claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Bourke in view of Barrenscheen.

(2) Rejection of claims 2-6 under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen.

Rejection of claim 10 under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen and Luo.

VII. ARGUMENT

I. Rejection of Claim 1

Appellant respectfully submits that claim 1 would not have been rendered obvious in view of the combination of Bourke and Barrenscheen because the combined references do not teach or suggest all of the features of the claims, and one skilled in the art would not have been motivated to modify the system of Bourke based on the teachings of Barrenscheen.

Claim 1 recites in part:

> wherein the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor.

The Examiner asserts that Barrenscheen discloses this feature of the claim and apparently reads the claimed multiplexer on Bus Interface (BI1) as disclosed by Barrenscheen.

Appellant respectfully submits that the Bus Interface BI1 is not a multiplexer. Instead, Bus Interfaces BI1-BI4 are used to connect the data transmission device DTU to the first through fourth buses BUS1-BUS4, respectively. Consequently, Bus Interface BI1 does not perform the functions of and is not described as a multiplexer in Barrenscheen.

The Examiner maintains that the claimed multiplexer reads on the Bus Interface (BI1), and asserts that:

> [T]he recited claiming language "multiplexer," and its function in the exemplary claim 1 are interpreted as the bus interface BI1 performs the functions of and is described as the claimed subject matter "multiplexer" in Barrenscheen.[1]

Appellant respectfully submits that claim 1 would not have been rendered obvious by Bourke and Barrenscheen. There is simply no disclosure of, nor has the Examiner provided specific support in Barrenscheen that the Bus interface, BI1 acts as or performs the functions of a multiplexer.

The Examiner also maintains that Barrenscheen discloses that BUS1 in FIGS. 2A-B is synchronized with the processor, and cites paragraph [0035] of Barrenscheen as allegedly disclosing this feature of claim 1. However, paragraph [0035] merely discloses that when the data transmission device (DTU) is used as a DMA controller, it can transmit data between devices connected to the same bus or between devices connected between different buses autonomously. Although the DTU which is used as a DMA in Barrenscheen may transfer data between BUS1 and BUS2 and between their respective devices, Barrenscheen does not require BUS1 and BUS2 be synchronized with the processor. Appellant respectfully submits that there is simply no disclosure in Barrenscheen that the BUS1 is synchronized with a processor.

For at least the foregoing reasons, Appellant respectfully submits that claim 1 is not rendered obvious in view of the combined teachings of Bourke and Barrenscheen.

[1] Page 17 of the Office Action dated January 18, 2007.

II. Rejection of claims 2, 4, and 10

With respect to independent claims 2, 4, and 10, the Examiner asserts that Masayuki teaches both a synchronous bus and an asynchronous bus as required by independent claims 2, 4, and 10 and cites bus 34 and bus 33 of Masayuki as allegedly respectively reading on the claimed synchronous and asynchronous buses.

Appellant respectfully submits that it appears that the Examiner is merely assuming that CPU bus 34 is (synchronous) synchronized with CPU 41, and that image data bus 33 is (asynchronous) not synchronized with CPU 41 because image data bus 33 is not directly connected to CPU 41 in Fig. 2. However, nowhere does Masayuki disclose that image data bus 33 is asynchronous. Moreover, Masayuki does not disclose any terms related to "synchronous" and "asynchronous".

The Examiner simply asserts that:

> Even though the Applicant argues that Masayuki does not disclose any terms related to 'synchronous' and 'asynchronous', Masayuki discloses CPU (i.e., processor) and CPU bus (i.e., synchronized bus with said CPU), and further, image data bus (i.e., asynchronous data bus) being synchronized by Sync Generator in the Signal Processor, not being synchronized with said CPU (i.e., processor).[2]

Appellant respectfully submits that claim 2 and analogous claims 4 and 10 would not have been rendered obvious over Masayuki.

[2] Pages 18-19 of the Office Action dated January 18, 2007.

First, there is simply no teaching or suggestion in Masayuki of synchronous and asynchronous buses. Masayuki teaches a method of preventing delays on an image data bus and improving signal processing efficiency by controlling/managing the read-out and write-in process of storage means connected to the image data bus. Nowhere does Masayuki expressly disclose synchronizing a data bus with a processor.

At best, Masayuki discloses that the sink generator 26 may provide a synchronization signal (for example a clock signal), not to the image bus 33, but only to the timing generator 13, wherein the timing generator 13 generates a horizontal synchronization signal and a vertical synchronization signal controlling every circuit of the image generator (see the signal lines of FIG. 1 and paragraphs [0014] and [0017]). In other words, the synchronization signal generated by the sink generator 26 is only for generating a horizontal synchronization signal and a vertical synchronization signal controlling every circuit of the image generator 10.

Appellant also respectfully submits that it appears that the image bus 33 is synchronized with CPU 41 as CPU bus 34, because the image bus 33 is directly connected to the CPU bus 34, not via a buffer, as illustrated in FIG. 2 of Masayuki. Therefore, the Examiner's assertion that image bus 33 is an asynchronous data bus not synchronized with the processor and synchronized with the sink generator is clearly erroneous.

Further, the fact that Masayuki teaches a signal processing unit which prevents delay of image data does not necessarily mean that this "inherently" teaches that the image data bus is synchronized with the CPU as alleged by the Examiner.[3]

Second, the comments in the Final Office Action regarding inherency are not understood; the principle of inherency is applicable only with respect to 35 U.S.C. §102 rejections. Inherency and obviousness are distinct concepts. A retrospective view of inherency is not a substitute for some teaching or suggestion that supports the selection and use of the elements in the particular claimed combination. In deciding that a novel combination would have been obvious, there must be a supporting teaching in the prior art; for that which may be inherent is not necessarily known, and obviousness cannot be predicated on what is unknown. See In re Newell, 13 U.S.P.Q.2d 1248, 1250 (Fed. Cir. 1989).

Further, Appellant submits that it is not inherent that image data bus 33 is (asynchronous) not synchronized with CPU 41 in Fig. 2, because evidence of inherency in a reference "must make it clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. USA Inc. v. Monsanto Co., 948 F.2d 1264, 1269 (Fed. Cir. 1991) (emphasis added). Additionally, "Inherency, however may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Id. Even if the prior art reference could have equally been used or made with only two possibilities,

[3] Page 19 of the Office Action dated January 18, 2007.

a patent claim which claims one of the two possibilities will not be anticipated because that limitation was not "necessarily" present in the prior art disclosure. See Finnigan Corp. v. I.T.C., 51 U.S.P.Q.2d 1001, 1009-10 (Fed. Cir. 1999) (holding that a prior art reference that disclosed a set-up for performing only resonance or nonresonance ejection was insufficient to show, clearly and convincingly, that nonresonance ejection was inherently taught by the prior art reference). Similarly, even if the image data bus 33 could either be synchronized or not synchronized with CPU 41, this possibility cannot be said to disclose that the image data bus is *necessarily* not synchronized when Masayuki is silent with respect to this feature.

As discussed above, Barrenscheen does not disclose whether or not BUS1 or BUS2 is synchronous. Further, Sodos and Luo do not compensate for the deficiencies of Barrenscheen and Masayuki to meet the particular requirements of independent claims 2, 4, and 10.

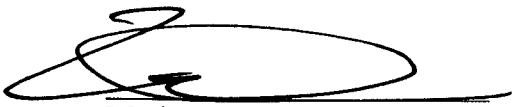
Even taken as a whole for what they would have meant to a skilled artisan, the individual or combined teachings of Masayuki, Barrenscheen, Sodos and Luo do not anticipate or render obvious the features of independent claims 2, 4, and 10

For at least the foregoing reasons, Appellant respectfully submits that claims 2, 4, and 10 are not rendered obvious in view of the combined teachings of Masayuki and Barrenscheen. Claims 3 and 5-9 should also be allowable at least by virtue of their dependency on independent claims 2 and 4.

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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WASHINGTON OFFICE
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Date: November 2, 2007

CLAIMS APPENDIX

CLAIMS 1-10 ON APPEAL:

1. (previously presented): A buffering apparatus comprising:

an asynchronous data bus write unit which, when control information indicating a request for writing in a buffer connected to an asynchronous data bus not synchronized with a processor is provided by a multiplexer connected to the processor, receives third data from the multiplexer, stores the third data, and transfers the stored third data to a second memory through the asynchronous data bus; and

an asynchronous data bus read unit which, when control information indicating a request for reading from the buffer is provided by the multiplexer, receives fourth data from the second memory through the asynchronous data bus, stores the fourth data, and transfers the stored fourth data to the multiplexer,

wherein the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor.

2. (previously presented): A processor bus connection method comprising:

(a) when address information indicating an address of a first memory connected to a synchronous data bus synchronized with a processor, from the processor is received, receiving first data from the processor and transferring the received first data to the first memory through

the synchronous data bus, or receiving second data from the first memory through the synchronous data bus and transferring the received second data to the processor; and

(b) when address information indicating an address of a second memory connected to an asynchronous data bus not synchronized with the processor, from the processor is received, receiving third data from the processor, transferring the third data, storing the transferred third data, and transferring the stored third data to the second memory through the asynchronous data bus, or receiving fourth data from the second memory through the asynchronous data bus, storing the fourth data, transferring the stored fourth data, receiving the transferred fourth data, and transferring the received fourth data to the processor.

3. (previously presented): The processor bus connection method of claim 2, wherein (a) comprises:

(a1) when the address information indicating the address of the first memory is provided by the processor and control information indicating a request for writing in the first memory is provided by the processor, receiving the first data from the processor and transferring the received first data to the first memory through the synchronous data bus; and

(a2) when the address information indicating the address of the first memory is provided by the processor and the control information indicating the request for reading from the first memory is provided by the processor, receiving the second data from the first memory through the synchronous data bus and transferring the received data to the processor.

4. (previously presented): A synchronous bus and asynchronous bus path method comprising:

(a) receiving input data and transferring the received input data through a synchronous bus synchronized with a processor;

(b) receiving the input data through the synchronous bus and transferring the received input data;

(c) generating first data or third data from the transferred input data and transferring the generated first or third data;

(d) receiving the first data, transferring the received first data to a first memory through the synchronous data bus, or receiving and storing the third data and transferring the stored third data to a second memory through an asynchronous bus not synchronized with the processor;

(e) receiving the first data through the synchronous bus and storing the first data; and

(f) receiving the third data through the asynchronous bus and storing the third data.

5. (original): The method of claim 4, further comprising:

(g) transferring second data through the synchronous bus;

(h) transferring fourth data through the asynchronous bus;

(i) receiving the second data through the synchronous bus and transferring the received second data, or receiving the fourth data through the asynchronous bus, storing the fourth data, and transferring the stored fourth data;

(j) generating output data from the second data or fourth data and transferring the output data;

(k) receiving and storing the output data and transferring the stored output data through the asynchronous bus; and

(l) receiving the output data through the asynchronous bus and outputting the received output data, or receiving the third data from the second memory through the asynchronous bus and outputting the received third data.

6. (original): The method of claim 5, wherein if the received output data or the received third data is display data, the received output data is displayed.

7. (original): The method of claim 5, further comprising:

(m) giving permission on the use of the synchronous bus; and

(n) giving permission on the use of the asynchronous bus.

8. (original): The method of claim 7, wherein in (a), the received input data is transferred through the synchronous bus for which permission to use is given in (m); in (b), the input data is received through the synchronous bus for which permission to use is given in (m); in (d), the received first data is transferred to the first memory through the synchronous data bus for which permission to use is given in (m), or the stored third data is transferred to a second memory through the asynchronous bus for which permission to use is given in (n); in (d), the first data is received through the synchronous bus for which permission to use is given in (m) and stored; and in (f), the third data is received through the asynchronous bus for which permission to use is given in (n) and stored.

9. (original): The method of claim 8, wherein in (g), the second data is transferred through the synchronous bus for which permission to use is given in (m); in (h), the fourth data is transferred through the asynchronous bus for which permission to use is given in (n); in (i), the second data is received through the synchronous bus for which permission to use is given in (m)

and the received second data is transferred, or the fourth data is received through the asynchronous bus for which permission to use is given in (n), stored, and the stored fourth data is transferred; in (k) the output data is received and stored, and the stored output data is transferred through the asynchronous bus for which permission to use is given in (n); and in (l), the output data is received through the asynchronous bus for which permission to use is given in (n) and the received output data is output to a user, or the third data from the second memory is received through the asynchronous bus for which permission to use is given in (n) and the received third data is output.

10. (previously presented): A tangible computer readable recording medium including a computer program having instructions for controlling a synchronous bus and asynchronous bus, the instructions comprising:

(a) receiving input data and transferring the received input data through the synchronous bus synchronized with a processor;

(b) receiving the input data through the synchronous bus and transferring the received input data;

(c) generating first data or third data from the transferred input data and transferring the generated first or third data;

(d) receiving the first data, transferring the received first data to a first memory through the synchronous data bus, or receiving and storing third data and transferring the stored third data to a second memory through an asynchronous bus not synchronized with the processor;

(e) receiving the first data through the synchronous bus and storing the first data; and

(f) receiving the third data through the asynchronous bus and storing the third data.

EVIDENCE APPENDIX:

There has been no evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or any other similar evidence.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.

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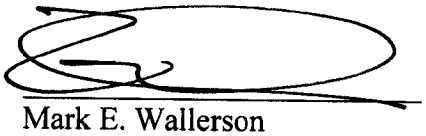
SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. The statutory fee of $510.00 is being charged to Deposit Account No. 19-4880 via EFS Payment Screen. The USPTO is also directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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